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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner:	Dr. Joseph D. Torres (parent)
Group Art Unit:	2133 (parent)
Application No.:	(new)
Filing Date:	October 23, 2003
Applicant(s):	Bruce E. Hayden et al

Invention:

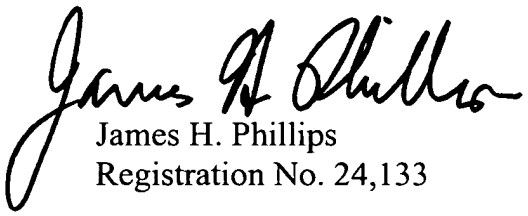
COMPUTER PROCESSOR READ/ALTER/REWRITE OPTIMIZATION CACHE INVALIDATE SIGNALS

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

PRELIMINARY AMENDMENT

The Divisional application filed herewith is in response to the Examiner's requirement for an election in the parent (09/752,924) hereof. The present application is exactly like the original execept for the new first paragraph on page 1 identifying the application as a Divisional of the parent and for the submission only of Claims 1-4 which correspond to original (in the parent) Claims 7-10; i.e., the non-elected claims to be prosecuted in this application.

Respectfully submitted,



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